This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. – 31. (Cancelled)

32. (Previously presented) A method comprising:
providing a substrate; and
providing a first strained layer disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm,
wherein the first strained layer is compressively strained.

33. (Previously presented) The method of claim 32, wherein the substrate comprises Si.

34. (Previously presented) The method of claim 32, wherein the first strained layer comprises Ge.

35. – 36. (Cancelled)

37. (Previously presented) The method of claim 32, wherein the first strained layer has a surface roughness of less than approximately 0.77 nm.

38. (Previously presented) The method of claim 32, further comprising providing an insulator layer disposed beneath the first strained layer.

39. (Previously presented) A method comprising:
providing a substrate;
providing an insulator layer over the substrate;
providing a first strained layer disposed above the substrate and the insulator layer, the first strained layer having an average surface roughness of no more than approximately 2 nm,
wherein the insulator layer comprises SiO_2.

40. (Previously presented) The method of claim 38, wherein the step of providing an insulator layer comprises wafer bonding.

41. (Previously presented) The method of claim 32, further comprising providing a relaxed layer disposed beneath the strained layer.

42. (Previously presented) The method of claim 41, wherein the relaxed layer has an average surface roughness of less than approximately 2 nm.

43. (Previously presented) The method of claim 42, further comprising planarizing the relaxed layer to reduce surface roughness.

44. (Previously presented) The method of claim 41, wherein the step of providing a relaxed layer comprises epitaxial growth.

45. (Previously presented) The method of claim 41, wherein the step of providing a relaxed layer comprises wafer bonding.

46. (Previously presented) The method of claim 41, wherein the relaxed layer comprises SiGe.

47. (Previously presented) The method of claim 46, wherein the substrate comprises a graded-composition SiGe layer.

48. (Previously presented) The method of claim 46, wherein the relaxed layer has an average surface roughness of less than approximately 0.77 nm.

49. (Previously presented) The method of claim 46, further comprising providing a regrown SiGe layer on the relaxed layer.

50. (Previously presented) The method of claim 49, wherein the regrown layer has a thickness of less than approximately 2 μm.

51. (Previously presented) The method of claim 49, wherein the regrown layer has a thickness of less than approximately 0.5 μm.

52. (Previously presented) The method of claim 49, wherein the regrown layer is substantially lattice-matched to the relaxed layer.

53. (Previously presented) The method of claim 32, further comprising providing a second strained layer disposed above the first strained layer.

54. (Previously presented) The method of claim 32, further comprising providing a spacer layer disposed above the first strained layer.

55. (Previously presented) The method of claim 54, wherein the spacer layer has a thickness of less than approximately 5 nm.

56. (Previously presented) The method of claim 54, wherein the first strained layer comprises Ge and the spacer layer consists essentially of Si.

57. (Previously presented) The method of claim 54, further comprising providing a second strained layer disposed above the spacer layer.

58. (Previously presented) The method of claim 57, further comprising providing a gate stack disposed above the second strained layer.

59. (Previously presented) The method of claim 54, wherein the spacer layer comprises Ge.

60. (Previously presented) The method of claim 54, further comprising providing a gate stack disposed above the spacer layer.

61. (Previously presented) The method of claim 60, further comprising providing supply layer dopants located in the spacer layer.

62. (Previously presented) The method of claim 61, wherein the supply layer dopants are provided by implantation.

63. (Previously presented) The method of claim 60, further comprising providing supply layer dopants located below the strained layer.

64. (Previously presented) The method of claim 63, wherein the supply layer dopants are provided by implantation.

65. (Previously presented) The method of claim 32, wherein the first strained layer has an average surface roughness of less than approximately 0.77 nm.

66. (Previously presented) The method of claim 32, further comprising providing a gate stack disposed above the first strained layer.

67. – 69. (Cancelled)

70. (Previously presented) The method of claim 66, further comprising providing metal silicide regions.

71. (Previously presented) A method comprising:

providing a substrate;

providing a first strained layer disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm;

providing a gate stack disposed above the first strained layer; and

providing metal silicide regions,

wherein the metal silicide regions comprise alloyed metal-SiGe.

72. (Previously presented) A method comprising:

providing a substrate;

providing a first strained layer disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm;

providing a gate stack disposed above the first strained layer; and

providing metal silicide regions,

wherein the metal is selected from the group consisting of: Ti, Co, and Ni.

73. (Previously presented) A method comprising:

providing a substrate;

providing a first strained layer disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm;

providing a gate stack disposed above the first strained layer; and

providing metal silicide regions,

wherein the step of providing metal silicide regions comprises deposition followed by annealing.

74. (Currently amended) A method comprising:

providing a substrate;

providing a first strained layer disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm;

providing a gate stack disposed above the first strained layer;

providing metal silicide regions; and

providing source and drain contact areas.

75. (Previously presented) The method of claim 74, further comprising providing an additional SiGe or Ge layer in the source and drain contact areas prior to providing metal silicide regions.

76. (Previously presented) The method of claim 75, further comprising providing an additional Si layer above the SiGe or Ge layer prior to providing metal silicide regions.

77. (Previously presented) The method of claim 32, wherein the step of providing the strained layer comprises epitaxial growth.

78. (Previously presented) The method of claim 32, wherein the step of providing the strained layer comprises wafer bonding.

79. (Previously presented) The method of claim 65, further comprising providing a gate stack disposed above the first strained layer.

80. (Previously presented) A method comprising:

providing a substrate;

providing a first strained layer disposed above the substrate, the first strained layer having an average surface roughness of no more than approximately 2 nm.

providing a gate stack disposed above the first strained layer; and

providing metal silicide regions,

wherein the first strained layer has an average surface roughness of less than approximately 0.77 nm.

81. (Previously presented) The method of claim 80, wherein the metal silicide regions comprise alloyed metal-SiGe.

82. (Previously presented) The method of claim 80, wherein the metal comprises Ni.

83. (Previously presented) The method of claim 80, further comprising providing source and drain contact areas.

84. (Previously presented) The method of claim 83, further comprising providing an additional SiGe or Ge layer in the source and drain contact areas prior to providing metal silicide regions.

85. (Previously presented) The method of claim 65, further comprising providing a relaxed layer disposed beneath the strained layer.

86. (Previously presented) The method of claim 85, wherein the relaxed layer comprises SiGe.

87. (Previously presented) The method of claim 80, wherein the first strained layer is tensilely strained.

88. (Previously presented) The method of claim 80, wherein the first strained layer is compressively strained.

89. (Previously presented) The method of claim 39, wherein the step of providing an insulator layer comprises wafer bonding.